REMARKS

Claims 1-24 are pending and stand rejected. The Examiner's reconsideration is respectfully requested in view of the above amendment and the following remarks.

On page 2 of the Office Action, the Examiner indicates that the Information Disclosure Statement filed on July 23, 2002 fails to comply with 37 C.F.R. 1.98(a)(1) because the Examiner is unable to locate a listing of references: JP10232775, EPO51148482, and EPO992894A1.

Applicant refers the Examiner's attention to Paper No. 4, wherein the above-cited references were listed in the IDS, Form 1449 filed on July 23, 2002. It can be seen from the Form 1449 that the prior Examiner had initialed next to the above-cited references on March 23, 2004. Therefore, these references have already been considered.

In paragraph 4 of the Office Action, the Examiner indicates that the Japanese JP62066344 (sic; it should be JP62063344) cannot be located and therefore has not been considered. Applicant submits that this reference was submitted together with the above three (3) cited reference considered by the prior Examiner and therefore Applicant believes that JP62063344 is in the file with the Examiner. In any event, a corresponding foreign search authority has indicated that JP62063344 is a reference of technical background. Therefore, Applicant believes that this reference does not affect the patentability of the present application and placement of this reference in the application file is sufficient.

In paragraph 5 of the Office Action, the Examiner objected to the title as not indicative of the invention to which the claims are directed.

The title has been changed to "Loop Instruction Processing Using Loop Buffer In A Data Processing Device Having A Coprocessor".

In Paragraph 6 of the Office Action, the Abstract of the Disclosure was objected to for minor informalities.

The Abstract has been amended as suggested by the Examiner.

In paragraph 7 of the Office Action, claim 20 was objected to because of informalities. The Examiner suggested changing "multiplexor" with --multiplexer--. Applicant notes that claim 20 as originally filed had "multiplexer" and such term was changed to "multiplexor" pursuant to suggestion by the Examiner in Paper No. 4. Applicant believes that either multiplexor or multiplexer is correct. In any event, "multiplexor" is now amended to --multiplexer-- pursuant to the present Examiner's suggestion.

In the drawings, amended Figure 1 is submitted herewith to correct typographical errors, i.e., "coprocessor" in box 120 and "program" in box 130. Approval of the correction is respectfully requested.

Claims 1-7, 14-16, 21, and 23-24 were rejected under 37 USC 103 as unpatentable over MacGregor in view of Kiuchi. The Examiner stated in paragraph 10 of the Office Action "MacGregor has taught a method for executing instructions using a CPU and a coprocessor (see Fig. 1)... comprising the steps of: A) decoding the coprocessor-type instructions by the coprocessor (see the abstract). B) MacGregor has not taught that if a loop operation is decoded, retrieving from the program memory the instructions within the loop... However, Kiuchi has taught such a concept....

Consequently, in order to save power in MacGregor's system, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify MacGregor's coprocessor to include Kiuchi's loop buffer. In addition, one of ordinary skill in the art would have recognized that this would also increase the efficiency of Macgregor because by storing instructions locally in a loop buffer within the coprocessor, they would be obtained much faster than if they had to be obtained fro an external source."

The rejection is respectfully traversed.

MacGregor discloses a device having a processor and a coprocessor and the use of a logical bus structure with the processors. MacGregor makes no reference to processing loop instructions. Kiuchi discusses the use of a data processor for processing loop instructions, but makes no reference to the use of any coprocessors. The Examiner cites power savings and processing efficiency as motivation to combine MacGregor to Kiuchi and also because Kiuchi taught that a data processor includes a loop buffer and MacGregor's coprocessor is a data processor. Applicant respectfully submits that power savings and processing efficiency are design goals in nearly every conceivable processing device and without more, one ordinary skilled in the art looking at a processing device having a CPU and a coprocessor to implement data processing using a logical bus would not look to a teaching on loop buffer processing, unless either MacGregor suggests or discusses problems with loop processing using such processing device or Kiuchi suggests or discusses improving processing of a loop instruction using a coprocessor and a logical bus. No such references can be found in

either MacGregor or Kiuchi. Therefore, Applicant respectfully submits that the combination of MacGregor to Kiuchi appear to be based on hindsight than on what the skilled artisan would have gleaned from the cited references.

Further, even assuming if MacGregor can be combined with Kiuchi, a prima facia case of obviousness cannot be established because all the claim limitations are not taught or suggested by MacGregor and/or Kiuchi. In particular, Applicant respectfully submits that the Examiner misinterpreted MacGregor as disclosing the step "decoding the coprocessor-type instructions by the coprocessor" as essentially claimed in claims 1, 14, and 24. The Examiner points to the Abstract of MacGregor as disclosing this step. The Abstract of MacGregor states, "the processor, upon encountering in its instruction stream an instruction having a particular Operation word format, will transfer a Command word following the Operation word to a particular Coprocessor designated by a Coprocessor Identity field in the Operation word." This passage in the Abstract of MacGregor makes clear that it is the processor and not the coprocessor which decodes the instructions. This process can also be seen from Figure 1 of MacGregor, wherein the decoder is shown as being fed with function code by the processor and not by the coprocessor. Therefore, MacGregor's device cannot "decode the coprocessor-type instructions by the coprocessor", as essentially claimed in claims 1, 14, and 24 of the present application. Kiuchi does not disclose a coprocessor, much less "decode the coprocessor-type instructions by the coprocessor", as essentially claimed in claims 1, 14, and 24 of the present application. Therefore, a prima facia case of obviousness

cannot be established because all of the claim limitations of the claims are not taught or suggested by the combined teaching of MacGregor and Kiuchi.

Accordingly, it is believed that claims 1, 14, and 24 are patentably distinct and not rendered obvious by MacGregor and/or Kiuchi. Reconsideration of the rejection is respectfully requested.

Claims 2-13 and 15-23 depend directly or indirectly upon claims 1 and 14, respectively. They are patentable in view of the cited references for the reasons discussed above for the independent claims.

Claims 8-13, 16-18, and 20 were also rejected under 35 USC 103 as unpatentable over MacGregor in view of Kiuchi and further in view of Moyer.

Claims 8-13 depend upon claim 1 and claims 16-18 and 20 depend upon claim 14. Moyer was cited as an additional reference for teaching a step of accessing flags in a loop buffer and multiplexing instructions using a loop buffer flag.

For the reasons discussed above, the combination of the several references to arrive at the claimed invention appear to be a hindsight reconstruction based on Applicant's teaching in the present application. Such combination is improper and therefore would not render the claims obvious. Further, Moyer fails to cure the deficiencies of MacGregor and Kiuchi with respect to the independent claims as discussed above. Accordingly, claims 8-13, 16-18, and 20 are not rendered obvious by MacGregor in view of Kiuchi and Moyer.

For the foregoing reasons, the above identified application including claims 1-24 is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully requested.

Respectfully submitted,

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